# Intel® 830 Chipset Family: 82830M / 83830MG / 82830MP Graphics and Memory Controller Hub (GMCH-M)

## Specification Update

*February 2005*

**Notice**: The Intel. 830 chipset family may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Reference Number: 298522-004

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# Revision History

| Rev | Draft/Changes | Date |
|---|---|---|
| -001 | Initial Release | October 2001 |
| -002 | Added Intel 830 Chipset Family Specification Clarification #1 | July 2002 |
| -003 | Added Intel 830 Chipset Errata #15, #16 | May 2003 |
| -004 | Added Intel 830 Chipset Family Specification Clarification #2, #3 | February 2005 |

# Preface

This document is an update to the specifications contained in the Intel® 830 Chipset Family GMCH M Datasheet (DRN:298338-003). It is intended for hardware system manufacturers. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes for the 82830MP discrete AGP graphic SKU and the 82830M and 82830MG internal graphics SKU's.

# Nomenclature

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

**Errata** are design defects or errors. Errata may cause the Intel 830MP GMCH-M behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

# Component Identification via Programming Interface

The Intel 830MP GMCH-M may be identified by the following register contents:

| Stepping | Vendor ID[1] | Device ID[2] | Revision Number[3] |
|---|---|---|---|
| A4 | 8086h | 3575h (Device #0)<br>3576h (Device #1) | 02h<br>02h |
| A6 | 8086h | 3575h (Device #0)<br>3576h (Device #1) | 04h<br>04h |

The Intel 830M GMCH-M may be identified by the following register contents:

| Stepping | Vendor ID[1] | Device ID[2] | Revision Number[3] |
|---|---|---|---|
| A5 | 8086h | 3575h (Device #0)<br>3576h (Device #1)<br>3577h (Device #2) | 03h<br>03h<br>03h |
| A6 | 8086h | 3575h (Device #0)<br>3576h (Device #1)<br>3577h (Device #2) | 04h<br>04h<br>04h |

The Intel 830MG GMCH-M may be identified by the following register contents:

| Stepping | Vendor ID[1] | Device ID[2] | Revision Number[3] |
|---|---|---|---|
| A5 | 8086h | 3575h (Device #0)<br>3577h (Device #2) | 03h<br>03h |
| A6 | 8086h | 3575h (Device #0)<br>3577h (Device #2) | 04h<br>04h |

**Notes**:

1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

# Component Marking Information

The Intel 830MP may be identified by the following component markings:

| Stepping | S-Spec | Top Marking | Notes |
|---|---|---|---|
| A4 | SL5P7 | FW82830MP | Production 82830MP GMCH-M |
| A6 | SL62F | FW82830MP | Production 82830MP GMCH-M |

The Intel 830M may be identified by the following component markings:

| Stepping | S-Spec | Top Marking | Notes |
|---|---|---|---|
| A5 | SL5P8 | FW82830M | Production 82830M GMCH-M |
| A6 | SL62D | FW82830M | Production 82830M GMCH-M |

The Intel 830MG may be identified by the following component markings:

| Stepping | S-Spec | Top Marking | Notes |
|---|---|---|---|
| A5 | SL5P9 | FW82830MG | Production 82830MG GMCH-M |
| A6 | SL62E | FW82830MG | Production 82830MG GMCH-M |

# Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed Intel 830 Chipset Family GMCH-M steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

## Codes Used in Summary Table

| | |
|---|---|
| o X: | o Erratum, Specification Change or Clarification that applies to this stepping. |
| o Doc: | o Document change or update that will be implemented. |
| o Fix: | o This erratum is intended to be fixed in a future stepping of the component. |
| o Fixed: | o This erratum has been previously fixed. |
| o NoFix: | o There are no plans to fix this erratum. |
| o (No mark) or (Blank Box): | o This erratum is fixed in listed stepping or specification change does not apply to listed stepping. |
| o Shaded: | o This item is either new or modified from the previous version of the document. |

# Specification Changes

The following Specification Change is classified based on the whether it is applied to the (I) Intel 830 Chipset Family (All 830 SKU's), (II) Intel 830M/MP Chipset (for AGP graphics) or (III) Intel 830M/MG Chipset (for internal graphics).

## I. Intel 830 Chipset Family Specification Changes (All 830 SKU's)

| NO. | Stepping | | | PLANS | SPECIFICATION CHANGES |
|---|---|---|---|---|---|
| | A4 | A5 | A6 | | |
| 1 | X | X | X | Doc | AC'97 Overrun/Underrun Failures With Default Request Grant Ceiling |
| 2 | X | X | X | Doc | Transitioning From Self-Refresh to Auto-Refresh When Exiting S3 Causes Memory Corruption to Occur |
| 3 | X | X | X | Doc | Reboot Failure Due to Memory Bus Contention After Reset |

## II. Intel 830M/MP Specification Changes (for Discrete AGP Graphics)

| NO. | Stepping | | | PLANS | SPECIFICATION CHANGES |
|---|---|---|---|---|---|
| | A4 | A5 | A6 | | |
| 4 | X | X | X | Doc | AGP Discard Timer Time Out Count Does Not Load Correct Default Value |
| 5 | X | X | X | Doc | Extremely Long Latencies on AGP Master Initiated Reads to DRAM |
| 6 | X | X | X | Doc | SBA Strobes Active Prior to Disabling and Re-Enabling of AGP Without Asserting PCIRST# May Cause Subsequent SBA (Side Band Address) Mode AGP Transactions to be Incorrectly Processed |

## III. Intel 830M/MG Specification Changes (for Internal Graphics)

| NO. | Stepping | | | PLANS | SPECIFICATION CHANGES |
|---|---|---|---|---|---|
| | A4 | A5 | A6 | | |
| 7 | X | X | X | Doc | HW Cursor Image Shows Flicker on First Line of Cursor While System Sets Resolution to 1280 x 1024 Pixels with 32 Bits Colors Running at 75 Hertz |
| 8 | X | X | X | Doc | SDRAM Protocol Violation occurred When IGD (Internal Graphics Device) and DRPM (Dynamic Row Power Management) Enabled |
| 9 | X | X | X | Doc | Legacy VGA 132 Column Modes Supports Show Visual Artifact on Screen |
| 10 | X | X | X | Doc | VGA Panning in Text Mode Causes Display Corruption |
| 11 | X | X | X | Doc | Polarity of V-Sync and H-Sync in DPMS (Display Power Management Signaling) Power Saving Modes cannot be Controlled |
| 12 | X | X | X | Doc | GMCH-M Supports Aysnchronous Flip Only Through Display A with Resolution Set to Higher Than 640 x 480 Pixels |
| 13 | X | X | X | Doc | GMCH-M does not Supports Aysnchronous Flip for Display B (Pipe B). |
| 14 | X | X | X | Doc | Function 1 of GMCH-M Maximum Latency Register (Device 2: Function 1: ADDRESS OFFSET 3Fh) Is Not a Copy of Function 0 of the Register |

# Errata

The following erratum is classified based on whether it is applied to the (I) Intel 830 Chipset Family, (II) Intel 830M/MP Chipset or (III) Intel 830 M/MG Chipset.

## I. Intel 830 Chipset Family Errata (All 830 SKU's)

| NO. | Stepping | | | PLANS | ERRATA |
|---|---|---|---|---|---|
| | A4 | A5 | A6 | | |
| 1 | X | | | Fixed | 3.3V Rail Power Up Before the 1.25V Rail Causes 3.3V IO Buffer Pre-driver to be in an Unknown State |
| 2 | X | | | Fixed | System Hangs When Dynamic Row Power Down (CKE#) Interacts with Self-Refresh Cycles |
| 3 | X | X | | Fixed | GMCH-M Internal Leakage from 1.25V Core to the 1.8V I/O Rail |

## II. Intel 830M/MP Chipset Errata (for Discrete AGP Graphics)

| NO. | Stepping | | | PLANS | ERRATA |
|---|---|---|---|---|---|
| | A4 | A5 | A6 | | |
| 4 | X | | | Fixed | Intel 830MP only Supports 1 Clock for DRAM to Exit Power Down Mode |
| 5 | X | | | Fixed | Self-Refresh During Entry to C3/C4/S1-M/S3 and During Intel SpeedStep Technology Transistion Causes Lost AGP Cycles on the System Memory Interface |
| 6 | X | X | X | NoFix | GBOUT Driven to An Un-deterministic State in S3 |

### III. Intel 830M/MG Chipset Errata (for Internal Graphics)

| NO. | Stepping | | | PLANS | ERRATA |
|---|---|---|---|---|---|
| | A4 | A5 | A6 | | |
| 7 | X | X | | Fixed | High Bandwidth Writes in Legacy VGA Mode May Cause Lockups |
| 8 | X | X | | Fixed | VGA Accesses to Aliased VGA I/O Addresses are Sent to Internal MMIO (Memory Mapped IO) Location |
| 9 | X | X | | Fixed | Slow DOS Mode During LVDS Panel Fitting (Panel Expansion) |
| 10 | X | X | | Fixed | Legacy VGA Modes on CRT Display Causes Horizontal Jitter |
| 11 | X | X | | Fixed | B000-BFFF Segment VGA Reads Come from A000-AFFF |
| 12 | X | X | | Fixed | GMCH-M Only Support 10 Bit VGA Decoding; This May Cause I/O Conflict in Windows* 2000 and Windows XP Which Assume 16 Bit Decoding |
| 13 | X | X | | Fixed | GMCH-M Graphics Display Corruption and Lockups During Asynchronous Flips |
| 14 | X | X | | Fixed | Mode switch from Mode 4 (CGA) to any other VGA Mode (i.e., 3, 12, or 13) can cause display lockup when enabling GMCH-M pixel doubling mode using greater than 1280 x 1024 panel size |
| 15 | X | X | X | NoFix | VGA Timing |
| 16 | X | X | X | NoFix | VGA Panning |

# Specification Clarifications

### I. Intel 830M/MG Specification Clarifications (for Internal Graphics)

| NO. | Stepping | | PLANS | SPECIFICATION CLARIFICATIONS |
|---|---|---|---|---|
| | A5 | A6 | | |
| 1 | X | X | Doc | VGA and Graphics Accelerator Concurrency |
| 2 | x | x | Doc | 480p and 1080i Progressive Scan Resolutions Not Supported on 830M, 830MG Platforms |
| 3 | x | x | Doc | SDRAM 512Mb System Memory Technology is Not Supported on 830 Chipset Family. |

# Documentation Changes

There are no documentation changes.

| NO. | Stepping | | PLANS | DOCUMENTATION CHANGES |
|---|---|---|---|---|
| | A4 | A5 | | |
| | | | | There are no documentation changes. |

# Specification Changes

## Intel 830 Chipset Family (for all 830 SKU's)

### 1 AC'97 Over-run/Under-run Failures With Default Request Grant Ceiling

**Problem:** When using AC'97, the default IOQ ceiling causes audio streams to experience intermittent sound loss.

**Implication:** The default setting for the IOQ does not work as expected.

**Workaround:** Program BIOS with new settings (Dev 0: Fn 0, Reg. 50-51h, bits 6:4 = 010b).

**Status:** Specification change.

### 2 Transitioning From Self-Refresh to Auto-Refresh When Exiting S3 Causes Memory Corruption to Occur

**Problem:** When transitioning from sleep state S3 to S0, the transition from self-refresh to auto-refresh has a delay

**Implication:** Without compensation for these missed refresh cycles, the data in main memory becomes corrupted.

**Workaround:** The BIOS restores Dev 0: Fn 0, Reg. 7C-7Fh from the CMOS as the last step for getting memory functionality on a resume from S3 state. During this step, the register bits 10:8 should be set to Fast refresh by programming a value of 111b. The Fast refresh mode should be kept enabled for at least ~130 us (15.6 us "Normal Refresh") or 280 us (7.8us "Normal Refresh"). Then switch the BIOS to Normal refresh mode by programming the bits to a normal run time value of 15.6us or 7.8 us. The amount of delay is based on the following formula for 133Mhz memory clock: (N/Fast) + ((64ms – lag – N)/Normal)) = ref 64; N = (ref64 x Fast x Normal – Fast (64 – lag)) / (Normal – Fast)

**Status:** Specification change.

## 3 Reboot Failure Due to Memory Bus Contention After Reset

**Problem:** System may potentially hang during POST after a memory read cycle is interrupted by a system hard/soft reset event. At reset, all SDRAM control signals are driven low, which places some SO-DIMMs into an unknown state, continuously driving the data bus. When rows are initialized and tested individually, the continuously driving DIMM can cause data read failures until it is initialized. This affects systems with more than one row of memory.

**Implication:** Certain types of memory devices may not properly reinitialize if a memory read cycle is interrupted by a system hard/soft reset event. There is a potential for a system hang during memory testing if the BIOS workaround is not implemented. The SV environment has tested memory modules from a number of third party vendors and only some have exhibited any issues that require BIOS modifications to resolve.

**Workaround:** The following workaround summary is for reference only. Please contact your Intel sales representative for full details regarding the sample workaround code (Intel 830M Chipset Family Memory Initialization Sighting Alert Rev 0.6 – June 15, 2001 – NDA).

During restart, ensure that all rows of memory have been initialized and a dummy read is performed on each row of all SO-DIMMs prior to any memory testing. The following is a summary of the recommended memory initialization sequence during restart.

1. Steps for JEDEC initilization for SDRAM devices during boot up:
    a. NOP command
    b. Pre-charge all banks (at least 200 us after NOP)
    c. 8 CBR refreshes (Auto Refresh)
    d. MRS command
    e. Set GMCH-M Mode Select bits back to NORMAL operation mode
    f. Perform a dummy memory read cycle
2. Repeat this sequence for all memory rows for all SO-DIMMs
3. Test all memory rows after JEDEC initialization sequence is done on all memory rows

**Status:** No Fix. Specification Change.

# Intel 830M/MP Chipset (for AGP Graphics)

### 4 AGP Discard Timer Time Out Count Does Not Load Correct Default Value

**Problem:** The AGP discard timer is loaded with the value 0 after reset, which causes performance degradation when doing AGP Frame reads. The register description must be updated to reflect the hardware default and correct default value that should be programmed.

**Implication:** The hardware default value of 0 would result in a very short delayed transaction discard time-out value and AGP Frame read performance is impacted if the correct default value of 1Fh is not loaded.

**Workaround:** Program timer with correct value (Device 0:Function 0, Reg. B2-B3h, bit 8:4 = 1Fh).

The register description for the AGP discard timer should be as follows:

| | |
|---|---|
| 8:4 | **AGP PCI1 Discard Timer Time-out Count. (RW)** These bits control the length of AGP/PCI1 Delayed Transaction discard time-out for the purpose of enhancing the system testability.<br>Default Value = 00h.<br>Program with Correct Value = 1Fh (31d) for a discard count of 1024d ([value+1]*32). |

**Status:** Specification change.

### 5 Extremely Long Latencies on AGP Master Initiated Reads to DRAM

**Problem:** When both PCI and AGP are performing continuous accesses to system memory, the GMCH may de-assert TRDY# forever.

**Implication:** In order to reduce the long latencies seen when PCI and AGP perform continuous accesses to system memory, PCI-to-DRAM read caching should be disabled to discard all pre-fetched and buffered data once the PCI read terminates.

**Workaround:** Disable read caching (Device 0: Function 0, Reg. B2h, bit 9 = 1h).

**Status:** Specification change.

## 6 SBA Strobes Active Prior to Disabling and Re-Enabling of AGP Without Asserting PCIRST# May Cause Subsequent SBA (Side Band Address) Mode AGP Transactions to be Incorrectly Processed

**Problem:** When disabling and then re-enabling AGP via the AGP Enable bit in 830MP GMCH-M's AGP Command Register (PCI configuration Offset A8h, bit 8) without asserting PCIRST#, the FIFO pointers used for SBA transfers may go out of sync. This happens because some portions of the logic controlling the FIFO pointers are reset by the AGP Disable event, but other portions are not. The result of the FIFO pointers going out of sync is that subsequent AGP commands sent over the SBA bus may be incorrectly processed. The nature of the incorrect processing is indeterminate. Reads may return wrong data. Writes may write to the incorrect location. Reads may be converted into writes and vice versa. Lengths may be corrupted or commands may be lost.

**Implication:** When using an SBA mode AGP graphics controller with 830MP, if INIT is used to restart the system under Windows 2000 without asserting PCIRST#, system hangs are possible. Windows 98 and Windows ME do not appear to be affected. This difference is apparently due to Windows 2000 disabling and re-enabling AGP on a warm restart, while Windows 98 and Windows ME do not appear to execute the disable/enable sequence. DOS-mode utilities that disable and then re-enable the GMCH-M's AGP Enable bit (for example, while looping on SBA mode AGP diagnostics) may fail and/or hang the system.

**Workaround:** During warm restart, BIOS should ensure that PCIRST# is asserted.

**Status:** No Fix. Specification change.

# Intel 830M/MG Chipset (for Internal Graphics)

### 7 HW Cursor Image Shows Flicker on First Line of Cursor While System Sets Resolution to 1280 x 1024 Pixels with 32 Bits Colors Running at 75 Hertz

**Problem:** 830M and 830MG hardware cursor at the lower right corner of the screen shows flicker on first line of cursor. This only happens when system sets resolution to 1280 x 1024 pixels with 32 bits colors running at 75 Hertz.

**Implication:** 830M and 830MG hardware cursor does not perform as planned under this setting.

**Workaround:** Use software cursor for this particular setting. Software cursor supports for this setting have been implemented in Intel® Extreme Graphics driver (version 2901 or later).

**Status:** Specification change.

### 8 SDRAM Protocol Violation when IGD (Internal Graphics Device) and DRPM (Dynamic Row Power Management) Enabled

**Problem:** SDRAM protocol is violated when a page open occurs to a particular bank without a subsequent page close (with a pre-charge cycle) prior to entering power down mode. After some time, the next memory access will cause a row activate to the same bank. The protocol violation only occurs when internal graphics is enabled. The failure requires dynamic row power management to be enabled with an active row count less than the total number of rows present on the system.

**Implication:** This failure will cause data mismatch.

**Workaround:** For 830M/830MG graphics SKU's: Leave Active Row Count (Device 0: Function 0, Address Offset Register 7C-7Fh, bit [26:24]) at default value (default value=000).

Enable timer based power management by programming the DRAM Idle Timer (Device 0: Function 0, Address Offset Register 78-7Bh, bit [18:16])

**Status:** Specification change.

### 9 Legacy VGA 132 Column Modes Supports Show Visual Artifact on Screen

**Problem:** When running applications that use the VGA engine to display 132 column modes, the attributes (color, blinking, etc.) can be displayed incorrectly. Attribute values from subsequent characters may be used for previous character. In addition, programs using DOS 132 Column modes may have erroneous characters repeated on the screen.

**Implication:** 830M/MG GMCH-M Legacy VGA 132 Column modes support does not function as expected.

**Workaround:** None available.

**Status:** Specification change. 132 column modes no longer supported.

## 10 VGA Panning in Text Modes Causes Display Corruption

**Problem:** When panning in legacy VGA text modes 0, 1, 3 or 7, the display can be corrupted with vertical black lines.

**Implication:** Minimal impact is expected as DOS-based text panning applications are not widespread at this time.

**Workaround:** None available.

**Status:** Specification change. VGA text panning is no longer supported

## 11 Polarity of V-Sync and H-Sync in DPMS (Display Power Management Signaling) Power Saving Modes cannot be Controlled

**Problem:** The polarity of the CRT V-Sync and H-Sync is active high during DPMS power savings states (D1-D3) regardless of the sync polarity setting during the D0 state.

**Implication:** It is expected that almost all monitors will not be affected. Going into a power savings state requires changes to the sync frequency and the polarity possibly. It is expected that monitors will recognize this change and scan for the new settings.

**Workaround:** None available.

**Status:** Specification change. Only Positive polarity for CRT VSYNC and CRT HSYNC will be supported during DPMS D1-D3.

## 12 GMCH-M Supports Asynchronous Flip Only Through Display A with Resolution Set to Higher Than 640 x 480 pixels

**Problem:** Running 2D Flip with Async flips enabled in low resolution mode (640 x 480) causes system hang. Display becomes corrupted when asynchronous flips are performed on Display B.

**Implication:** System becomes unstable when Aysnc flip is enabled either on Display A with a low resolution (640 x 480) or on Display B.

**Workaround:** None Available.

**Status:** Specification change. Async flips not supported for Display A running in low-resolution mode (below 640 x 480) and Display B running any mode.

## 13 GMCH-M does not Supports Asynchronous Flip on Display B (pipe B)

**Problem:** Display becomes corrupted when Asynchronous flips are performed on Display B.

**Implication:** System becomes unstable when Asynchronous flips are enabled on Display B.

**Workaround:** None Available.

**Status:** Specification change. Asynchronous flips not supported for Display B running any mode.

## 14 Function 1 of the GHCH-M Maximum Latency Register (Dev 2:Fun1 Offset 3Fh) is Not a Copy of Function 0 of the Register

**Problem:** Function 1 and Function 0 of the 830M/MG GMCH-M Maximum Latency Register (Device 2: Function 1: Offset 3Fh) do not contain the same value.

**Implication:** 830 Chipset Family Datasheet contains incorrect description for Maximum Latency Register. Please see updated information below.

**Workaround:** Currently not available

**Status:** Specification change. Device 2: Function 1:Register 3F is not an exact copy of the same register Device#2:Function 0: Register 3F.

### MAXLAT—Maximum Latency Register - Device #2

Address Offset: 3Fh
Default Value: 00h (Function 0)
UNDEFINED (Function 1)
Access: Read Only
Size: 8 bits

The value returned for Device 2 Function 1 is UNDEFINED. The value returned for Device Function 0 is correct (00h).

| Bit | Description |
|---|---|
| 7:0 | **Maximum Latency Value.** Bits[7:0]=00h. The IGD has no specific requirements for how often it needs to access the PCI bus. |

# Errata

## Intel 830 Chipset (for all 830 SKU's)

### 1. 3.3V Rail Power Up Before the 1.25V Rail Causes 3.3V IO Buffer Pre-driver to be in an Unknown State

**Problem:** DDC1_CLK, DDC1_DATA, IC2_CLK, I2C_DATA, DDC2_CLK, DDC2_DATA, AGPBUSY#, VSYNC and HSYNC IO buffer pre-driver are in an unknown state when applying power to the 3.3V power rail before the 1.25V core rail is powered on.

**Implication:** When the 3.3V rail is powered on before the core rail, the IO buffer pre-drivers are in an unknown state causing high current on the 3.3V rail. This will result in excessive heat on the part if 3.3V rail is applied without cycling the 1.25V core rail.

**Workaround:** Cycle 1.25Vcore power rail within 200 ms after applying power to the 3.3V rail.

**Status:** Fix in A5 stepping verified

### 2. System Hangs When Dynamic Row Power Down (CKE#) Interacts with Self-Refresh Cycles

**Problem:** A boundary condition exits in GMCH-M that causes an internal conflict in the memory controller when a self-refresh command cycle collides with a power down mode (DRPM) cycle. SDRAM rows are already in a power down state due to a DRPM. The GMCH-M assumes that the system memory has entered the self-refresh state when this is not the case.

**Implication:** Memory corruption and system hang are possible results upon exit from the low power state.

**Workaround:** Please contact your Intel sales representative for details regarding the sample code (Intel 830M GMCH-M A4 DRPM/Self Refresh Workaround Reference Code rev 1.0 – July 2001 – NDA).

**Status:** Fix in A5 stepping verified.

### 3. GMCH-M Internal Leakage from 1.25V core to the 1.8V I/O Rail

**Problem:** If the 1.25V core rail powers up before the 1.8V rail, a leakage path exists until the 1.8V rail is powered up.

**Implication:** This leakage is negligible and will not affect GMCH-M operation.

**Workaround:** Power up 1.8V rail as soon as 1.25V rails is ramping up.

**Status:** Fix in A6 stepping verified.

### 4. Intel 830MP only Supports 1 Clock for DRAM to Exit Power Down Mode.

**Problem:** 2 CLK cycles required for the DRAM to exit from power down mode while GMCH-M support only 1 CLK cycle for exit from power down mode.

**Implication:** PC133 SDRAM spec requires 2 clocks for DRAM to exit power down mode. Most memory vendors support 1 CLK cycle by default.

**Workaround:** Use SO-DIMMs that support 1 clock cycle.

**Status:** Fix in A5 stepping verified.

### 5. Self-Refresh During Entry to C3/C4/S1-M/S3 and During Intel® SpeedStep™ Technology Transition Causes Lost AGP Cycles on the System Memory Interface

**Problem:** During entry into the C3, C4, S1M, or S3 low power state, and during entry into an Intel® SpeedStep™ Technology transition, the GMCH-M will attempt to put the SDRAMs into self-refresh mode 1.9 us after STP_AGP# assertion. In the unlikely event that AGP transactions are still pending in the GMCH's internal AGP buffer at that time, the current AGP transaction may be lost in the GMCH-M, resulting in no corresponding transaction on the SDRAM bus. (This scenario is unlikely because all known Mobile AGP controllers stop initiating new cycles on the AGP interface within 1 usec after STP_AGP# assertion; and these cycles will usually be completed before 1.9 us has elapsed since STP_AGP# assertion.) If the last pending cycle that is currently in progress when the self-refresh command begins is a read cycle, it may complete on the AGP interface, but the data may be corrupted. If the last pending cycle is a write cycle, it will not be completed on the system memory interface and internally will be lost.

**Implication:** Failures have only been seen in Intel's SV environment using special AGP test cards. Graphics cards from major vendors, including all known mobile AGP controllers, have been tested and no failures have been observed.

**Workaround:** Please contact your Intel sales representative for details regarding the sample code (Intel 830M GMCH-M A4 DRPM/Self Refresh Workaround Reference Code rev 1.0 – July 2001 – NDA).

**Status:** Fix in A5 stepping verified

### 6. GBOUT Driven to An Un-deterministic State in S3

**Problem:** GBOUT is driven to an undetermined state in the S3 sleep state.

**Implication:** This may cause a leakage issue on the platform.

**Workaround:** GBOUT – place a 0.01 uF series cap within 0.5 in of GBOUT on GMCH-M and a 240K pull-down within 0.5 in of CK-408.

**Status:** Documentation change

# Intel 830M/MG Chipset (for Internal Graphics)

### 7. High Bandwidth Writes in Legacy VGA Mode May Cause Lockups

**Problem:** Display lockup may occur if a VGA application tries to do a large amount of writes to the VGA memory space. The internal render cache is not properly flushed when a VGA writes occurs. If an application does a large number of writes, a pending write can be in the cache when VGA does a display read fetch. This results in a FIFO pointer updating improperly. If this occurs at the end of a display line, the VGA state machine may lock up due to these unsynchronized pointers.

**Implication:** This sighting was uncovered in an SV test environment. No failure has been identified with normal DOS applications, games, or otherwise and no issues have been reported to Intel. Text modes are NOT affected. High bandwidth, legacy VGA modes, such as Mode 12 and Mode X could be affected.

**Workaround:** None available.

**Status:** Fix in A6 stepping verified.

### 8. VGA accesses to aliased VGA I/O addresses are sent to internal MMIO (Memory Mapped IO) location

**Problem:** If any IO access with the lower 10 bit of the address matches the VGA IO address space would be translated into the GMCH MMIO space. If an aliased VGA I/O address corresponds to an existing GMCH-M MMIO offset address, the transaction will used the actual MMIO register. If the aliased VGA I/O address does not correspond to an existing MMIO address, then reads will return 00h and writes will be ignored.

**Implication:** Most registers offsets that would match this requirement are reserved and not implemented, thus effectively ignoring the transaction. The only range that will respond are some of the MMIO palette access registers, located at MMIO offset 0x0A000 through 0x0AFFF. For example, VGA I/O address 0xA3DA would be translated into MMIO offset 0x0A3DA and would access GMCH palette entry 246. If written, this would cause corrupted colors on any high resolution or VGA mode that uses the palette or gamma correction.

**Workaround:** None available.

**Status:** Fix in A6 stepping verified.

### 9. Slow DOS Mode During LVDS Panel Fitting (Panel Expansion)

**Problem:** When running Panel Fitting modes (expansion), frame-rate intensive DOS applications will run very slow due to limited CPU bandwidth to frame buffer.

**Implication:** Frame rate intensive DOS games in Panel Fitting mode will be slow and user will notice degradation in game play. This affects all legacy VGA modes. Windows Safe Mode will also exhibit slowness.

**Workaround:** Below settings have been found to provide the best compromise between speed and size when panel expansion is enabled.

For 1024 x 768 panels: All legacy VGA modes will have resolution size set to 800 x 600 pixels and will be centered on panel.

For 1400 x 1500 panels: All legacy VGA modes will have resolution size expanded to 1280 x 1024 pixels and will be centered on panel.

This workaround has been implemented in Video BIOS rev 2434 or later.

**Status:** Fix in A6 stepping verified.

### 10. Legacy VGA Modes on CRT Display Causes Horizontal Jitter

**Problem:** When running on a CRT with the VGA timing engine, the HYSNC width is inconsistent which causes extreme jitter in all VGA modes.

**Implication:** CRT image quality is noticeably reduced. The amount of jitter observed is monitor dependent.

**Workaround:** When running CRT only display, all legacy VGA modes will be displayed with 800 x 600 pixels mode timings resolution. This will result in the display being centered with a boarder and the size will depend on the VGA mode.

**Status:** This workaround has been implemented in video BIOS revision 2434 or later.

### 11. B000-BFFF segment VGA reads come from A000-AFFF

**Problem:** When VGA memory access is set to both the A000 and B000 segments (with VGA register GR06), read from B000 segment will come from A000 segment. The failure has been observed in Restart to DOS mode/ Startup Disk support in the Korean Windows 98/ME operating system due to a TSR BIOS (MSHBIOS.com) Similar corruptions has also been observed in DOS programs running in full screen mode in Korean Windows XP. For this failure, the screen shows as completely black or as corrupted characters although the system is still active.

**Implication:** Applications that attempt to read from B000 segment will find that they cannot read the data. The actual data returned will come from the A000 segment under this condition. VGA applications do not generally use both A000 and B000 at the same time.

**Workaround:** None available.

**Status:** Fix in A6 stepping verified.

### 12. GMCH-M Only Supports 10 bit VGA decoding; This May Cause I/O Conflicts in Win2K/XP Which Assume 16 Bit Decoding

**Problem:** PCI devices requesting I/O resources can fail with GMCH-M Internal Graphics on Windows 2000 / XP if the OS assigns an aliased VGA address. The 830M/MG decodes 10 bits only for VGA I/O access, similar to the AGP bus, to allow for true VGA legacy aliasing. Window 2000 and XP require 16-bit decoding for PCI devices, thus causing a conflict as they assume aliased addresses are passed to the PCI bus. Windows 95/98/ME OS are not affected as these OSes reserve aliased VGA address and will not assign them to PCI devices.

**Implication:** Windows 2000 and Windows XP will assign IO resources to third party vendors (i.e. Wireless mini-PCI Lan card) which should be reserved for VGA address space due to GMCH-M not decoding the full 16 bit address space. The operating system shows an IO conflict and the third party vendor cannot use space that the OS has assigned to it.

**Workaround:** The following workaround summary is for reference only. Please contact your local FAE for full details regarding the sample workaround code ( Intel 830M Legacy VGA I/O Alias Workaround Reference Code for ACPI OS's rev 0.25.)

For an ACPI OS, the solution is to report all the VGA Alias I/O address as conditionally consumed using standard ASL Design practices. The ranges should be reported as consumed if either Windows 2000 or Windows XP is detected and Device#2 is enabled.

Please follow these steps when implementing the workaround:

- Write ASL code to determine which OS is loaded.
- Write ASL code to determine whether Device# 2 is "ENABLED"
- In ASL, define a Generic Motherboard Device with a Current Resource Settings Method (_CRS) and a Status Method (_STA). The _CRS should report all the VGA Alias I/O Addresses and the _STA should correctly report if the device is decoding its resources.

**Status:** Fix in A6 stepping verified.

### 13. GMCH-M Graphics Display Corruption occur during Asynchronous Flips

**Problem:** When asynchronous flips are performed on Display A in resolution higher than 640 x 480 pixels, corruption have been observed.

**Implication:** Display is momentarily corrupted until screen has refreshed.

**Workaround:** Software workaround has been implemented in Intel® Extreme Graphics driver to hide corruption (version 2901 or later). Driver will detect A5 or A6 and not apply SW workaround for A6.

**Status:** Fix in A6 stepping verified.

### 14. Mode Switch from Mode 4 (CGA) to any other VGA Mode (ie 3, 12 or 13) can Cause Display Lockup with Pixel Doubling Mode is enabled using greater than 1280 x 1024 Panel Size

**Problem:** When initiating a mode switch: CR09, bit 7 and/or CR 17, bit 2 are toggled from a ONE (pixel double ON) to a ZERO (pixel scan OFF). This has a 50% chance of causing a lockup in the VGA display state machine. When lockup occurs, the display engine does not update a row counter due to an un-reset flip-flop. The failure generally results in one line of the display being repeated for the entire screen. This occurs on flat panels greater than 1280 x 1024, using the Intel 830 VGA pixel doubling method for panel fitting.

**Implication:** There is a limited real-world impact as very few applications use the CGA modes. Other non-standard modes could use the bits but Intel has not identified any application so far. Platforms using 1024 x 768 flat panels will not be impacted, as VCH will be used for panel fitting.

**Workaround:** VBIOS sets pixel doubling OFF before mode switch call occurs.

**Status:** Fix in A6 stepping verified.

### 15. VGA Timing

**Problem:** Some VGA applications, running in 40-column modes, that use a non-black border color, may experience color/visual issues on systems configured with certain monitors

**Implication:** 40-column VGA modes may experience visual color anomalies on some CRT monitors. This was observed using VGA focused Intel test software. With certain monitors, colors in active areas may change as the border color changes. As observed while using the test software, visual color anomalies can range from a slight color change difference to a blank screen. Based on the lack of customer or end user reported issues related to this erratum, the number of VGA applications that run in 40-column modes and also use non-black border colors is low. Based on Intel's validation and compatibility testing, the number of CRT monitors that exhibit this color anomaly is also low.

**Workaround:** No workaround exists.

**Status:** This will not be fixed in future steppings.

## 16. VGA Panning

**Problem:** VGA text mode diagnostic and stress test applications that use pixel panning can experience temporary visual anomalies under certain memory configurations. The memory configurations affected are 64 MB technology products that use 2-kB and 4-kB page sizes.

1. Test applications using a single VGA font table with a 32-kB font buffer range could fail. This failure was seen in a diagnostic utility.

2. Test applications using multiple VGA font tables could fail if the first two fonts are from different tables. This failing condition can occur in any memory configuration. This failure was seen in a stress test utility.

**Implication:** Entire scanlines will appear to flicker in some VGA diagnostic and stress test applications. However, there are no known customer sightings of this erratum. No known end user applications fail for this erratum.

**Workaround:** No workaround exists.

**Status:** This will not be fixed in future steppings.

# Specification Clarifications

## Intel 830M/MG Chipset (for Internal Graphics)

### 1. VGA and Graphics Accelerator Concurrency

The Intel 830M/MG Chipset does not support VGA memory accesses during graphics accelerator operations, such as BLTS and 3D activity. The Intel Extreme Graphics driver is written in a manner that will control VGA and high-resolution graphics interaction such that the activity will remain exclusive.

### 2. 480p and 1080i Progressive Scan Resolutions Not Supported on 830M, 830MG Platforms

The Intel 830M/MG does not support progressive scan of resolutions 480p and 1080i. This change affects Section 5.5.2.5.4 of Intel 830 Chipset Family: 82830 Graphics and Memory Controller Hub (GMCH-M) Datasheet (Document No: 298338). Any text stating support for these progressive scan resolutions should be ignored.

### 3. SDRAM 512Mb System Memory Technology is Not Supported on 830 Chipset Family.

Due to no availability of SDRAM 512Mb System Memory Technology during 830 Chipset Family product validation, SDRAM 512Mb Technology is not supported. This change affects Section 2.4 of Intel 830 Chipset Family: 82830 Graphics and Memory Controller Hub (GMCH-M) Datasheet (Document No: 298338). Any text stating support for SDRAM 512Mb Memory Technology should be ignored.

# Documentation Changes

There are no documentation changes.